IN THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently Amended) An intermediate semiconductor device fabrication structure comprising: an electronic chip component having all electrodes formed on one surface thereof, ~~a side wall~~ side walls thereof being covered with a protective material, and wherein there is substantially no protective material located on ~~the~~ one surface of the chip where all the electrodes are formed and further wherein the protective material on the side walls ~~wall~~ and a surface of the chip opposite the surface where the electrodes are located have been grinded or polished to a common level and the one surface of the chip where all the electrodes are formed is secured to an adhesive sheet and a plurality of additional same or different electronic chip components also have there respective sides where all the electrodes are formed secured to the adhesive sheet with the protective material located therebetween, and wherein the plurality of chip components are not from a same semiconductor wafer .

2. (Previously Presented) The electronic chip component according to claim 1 wherein said protective material comprises either one of an organic insulating resin and an organic insulating material.

3. (Previously Presented) The electronic chip component according to claim 1, comprising a semiconductor chip diced at a position of said protective material for mounting on a packaging substrate, wherein all of said side wall is covered with said protective material.

4. (Previously Presented) The electronic chip component according to claim 3, wherein a solder bump is formed on each of said electrodes.

5. (Canceled)

6. (Currently Amended) A pseudo wafer comprising a plurality of same or different electronic chip components each having all electrodes formed on one surface thereof~~,~~ which are bonded to each other with a protective material coated on side walls therebetween, and wherein there is no protective material located on the one surface of the chip where all the electrodes are formed and further wherein the protective material on the side wall and a surface of the chip opposite the surface where the electrodes are located have been grinded or polished to a common level and further wherein the plurality of chip components are not originally from a same semiconductor wafer.

7. (Original) The pseudo wafer according to claim 6, wherein said protective material comprises either one of an organic insulating resin and an inorganic insulating material.

8. (Previously Presented) The pseudo wafer according to claim 6, wherein said pseudo wafer is diced into a single semiconductor chip at a position of said protective material for mounting on a packaging substrate.

9. (Previously Presented) The pseudo wafer according to claim 8, wherein a solder bump is formed on each of said electrodes.

Claims 10-20 (Canceled) Claims 1-20 were previously canceled.